WHAT IS CLAIMED IS:

1. A thin film transistor array panel used for a liquid crystal display, comprising:

a gate line and a gate electrode formed on a substrate;

a gate insulating layer covering the gate line and the gate electrode;

a semiconductor layer formed on the gate insulating layer;

a data line, a source electrode and a drain electrode formed on the semiconductor layer;

a passivation layer covering the data line and the source electrode, and a part of the drain electrode; and

a pixel electrode connected to the exposed drain electrode, wherein the semiconductor layer has the same as the passivation film except a portion under the drain electrode, which is not covered with the passivation film.

2. The thin film transistor array panel of claim 1, further comprising a light shielding film formed on the passivation film in the same pattern as the passivation film.

3. The thin film transistor array panel of claim 1, wherein the light shielding film is made of opaque

material.

4. The thin film transistor array panel of claim 3, wherein the gate insulating layer is formed in the same pattern as the semiconductor layer, and the passivation film also covers the gate line and the gate electrode.

5. The thin film transistor array panel of claim 4, wherein the pixel electrode overlaps the gate line via the gate insulating layer, the semiconductor layer and the passivation film.

6. The thin film transistor array panel of claim 4, further comprising a conductive connection portion formed between the semiconductor layer and the passivation film covering the gate line, and wherein a part of the conductive connection portion is exposed outside the passivation film and is connected to the pixel electrode.

7. The thin film transistor array panel of claim 1, wherein the drain electrode is covered with the passivation film as a whole, and the passivation film has a contact hole which exposes a central portion of the drain electrode and through which the pixel electrode and the drain electrode are connected.

8. The thin film transistor array panel of claim 1, further comprising a doped semiconductor layer formed between the semiconductor layer, and the data line, the source electrode and the drain electrode, and formed in the same pattern as the data line, the source electrode and the drain electrode.

9. A method for manufacturing a thin film transistor array panel used for a liquid crystal display, comprising the steps of:

forming a gate line and a gate electrode by depositing a first conductive film on a substrate and etching through a photolithography process;

depositing an insulating layer and a semiconductor layer thereon;

forming a data line, and a source and a drain electrodes by depositing a second conductive layer and etching the photolithography process;

depositing an insulating layer on a whole surface;

depositing a passivation film covering the data line, the source electrode and a part of the drain electrode by patterning the insulating layer;

etching the semiconductor layer, using the passivation film as a mask; and

forming a pixel electrode by depositing a transparent conductive film and etching to contact the drain electrode.

10. The method of claim 9, further comprising the steps of depositing a light shielding film after

depositing the insulating layer, and etching the light shielding film through the photolithography process, wherein the insulating layer is patterned, using the etched light shielding film as a mask.

11. The method of claim 9, further comprising the steps of depositing a light shielding film before depositing the insulating layer, and patterning the light shielding film, wherein the light shielding film is patterned, using the patterned light shielding film as a mask.

12. The method of claim 9, wherein the passivation film is made of opaque material.

13. The method of claim 12, wherein the passivation film covers also the gate line and the gate electrode.

14. The method of claim 13, further comprising the step of etching the insulating layer, using the etched semiconductor layer as the mask.

15. The method of claim 14, wherein the etched second conductive film has a connection portion formed to overlap a part of the gate line.

16. The method of claim 15, wherein a part of the connection portion is exposed outside the passivation film and connected to the pixel electrode.

17. A method for manufacturing a thin film transistor array panel used for a liquid crystal display, comprising the steps of:

forming a gate line, a gate electrode and a gate pad by depositing a first conductive film on a substrate and etching through a photolithography process;

depositing an insulating layer and a semiconductor layer thereon;

forming a data line, and a source electrode, a drain electrode, and a data pad by depositing a second conductive layer and etching the photolithography process;

depositing an insulating layer on a whole surface;

forming a passivation film covering the gate and the data lines, the gate and the source electrodes, the gate and the data pads, and the drain electrode by patterning the insulating layer, and exposing the gate pad, the data pad and a part of the drain electrode;

etching the semiconductor layer and the insulating layer, using the passivation film, the exposed data pad and the exposed drain electrode as a mask; and

forming a pixel electrode by depositing a transparent conductive film and etching to contact the drain electrode.

18. The method of claim 17, wherein the transparent conductive film includes portions which cover the exposed gate pad and the exposed data pad respectively.

19. The method of claim 17, wherein the first conductive film is formed by two layers, that is, an upper layer and a lower layer.

20. The method of claim 18, wherein the lower layer of the first conductive film is made of Al, or of an Al alloy, and the upper layer of the first conductive film is made of Mo.

21. The method of claim 18, wherein the lower layer of the first conductive film is made of Cr, and the upper layer of the first conductive film is made of Al, or of an Al alloy.

21. The method of claim 21, further comprising the step of etching the upper layer of the first conductive layer, using the etched insulating layer as the mask after etching the gate insulating layer.